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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,105	03/16/2001	Noriaki Sakamoto	10417-066001	9488

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CHRIS T. MIZUMOTO
Fish & Richardson P.C.
Suite 2800
45 Rockefeller Plaza
New York, NY 10111

EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/810,105	Sakamoto et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jun 7, 2001

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-16 is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-16 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 11 recites the limitation "said conductive film" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1, 4, 6, 7, 10 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Fukutomi et al (US Pat. 5976912).

Regarding claim 1, Fukutomi et al disclose a semiconductor device comprising:

- a plurality of conductive paths (63/64, central die pad/support region and 69 in Fig. 22g) which are electrically separated from one another by a trench (66 in Fig. 22a-g)

- a semiconductor chip (65 in Fig. 22g) fixed on a first conductive path (central die pad/support region-not numerically referenced in Fig. 22g) having a die pad shape of the plurality of conductive paths

- connecting means such as metallic wires (67 in Fig. 22g) connecting bonding electrode of the chip and a second conductive path having a bonding shape pad/pattern (64 in Fig. 22a-g; Col. 22, line 33)

- an insulating resin/bonding material covering the chip being embedded in the trench among the plurality of conductive paths (68/66 in Fig. 22a-g) and integrally supporting the conductive paths with their rear surface being exposed

- the second conductive path (64 region outside the edge portion of the chip in Fig. 22a-g) being formed outside the chip and an external connecting pad (69 in Fig. 22f/g) is provided through the wiring extended from the second conductive path to the rear surface of the chip

(Fig. 22g; Fig. 22a-g; Col. 22, line 25- Col. 24, line 10).

Regarding claim 4, Fukutomi et al disclose the first conductive path coupled with the chip through a conductive material/layer (64 in Fig. 22a-g).

Regarding claim 6, Fukutomi et al disclose the insulating/bonding material (68/66 in Fig. 22 g) being provided over the entire region of the rear surface of the chip.

Regarding claim 7, Fukutomi et al disclose the connecting means such as metallic wires (67 in Fig. 22g).

Regarding claims 10 and 11, Fukutomi et al disclose the upper surface of the conductive path (63 in Fig. 22a-g) being covered with a different metallic material/film (64 in Fig. 22a-g) such as nickel, gold, etc (Col. 23, line 28).

5. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being anticipated by Kweon et al (US Pat. 5900676).

Regarding claims 14 and 16, Kweon et al disclose a semiconductor device comprising:

- a plurality of conductive paths (40, 120, 24, 22, etc. in Fig. 15) which are electrically separated from one another by a trench (Fig. 15)

- a semiconductor chip (110 in Fig. 15) directly connected with the conductive paths (120, 40, etc. in Fig. 15)

- an insulating resin/molding resin (140 in Fig. 15) covering the chip being embedded in the trench among the plurality of conductive paths and integrally supporting the conductive paths with their rear surfaces being partially exposed from the resin, and

- conductive paths (40/24 in Fig. 15) being connected with the chip at an external position of a periphery of the chip and extended to the rear surface of the chip to be an external terminal (Fig. 15; Col. 7, line 1- 42).

Regarding claim 15, Kweon et al disclose the chip being connected with the conductive path through bonding wires (130 in Fig. 15).

Regarding claim 16, Fukutomi et al disclose the semiconductor chip (110 in Fig. 15) being directly connected with the conductive paths (120/40 in Fig. 15).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 3, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al (US Pat. 5976912).

Regarding claim 2, as explained above for claim 1, Fukutomi et al further disclose the first conductive path (central die pad/support region-not numerically referenced in Fig. 22g) having smaller size than that of the rear surface of the chip and a third conductive path having a shape of an external connecting pad (69 in Fig. 22f/g; Col. 23, line 55) provided through the wiring extended from the second conductive path to the rear surface of the chip but fail to specify the third conductive path having a larger size than that of the second conductive path.

Fukutomi et al further disclose forming the wiring patterns/islands and external connecting pads using conventional photo resist processing and solder printing (Col. 22, line 33; Col. 23, line 55). It is a matter of a design choice to select the dimensions/shape of the wiring/electrode layers such as length/width, pad/island area, thickness, etc. of in chip packaging and interconnection technology art to achieve the desired electrical resistance and bonding yield.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the size of third conductive path being larger size than that of the second conductive path to achieve the desired electrical resistance and bonding yield in Fukutomi et al's device.

Regarding claim 3, Fukutomi et al disclose the third conductive path (69 in Fig. 22f/g; Col. 23, line 55) provided between the periphery of the chip and the first conductive path but fail to specify the second conductive path being in the form of an island.

As explained above for claims 1 and 2, Fukutomi et al disclose forming the wiring patterns/islands and external connecting pads using conventional photo resist processing and solder printing (Col. 22, line 33; Col. 23, line 55). It is a matter of a design choice to select the dimensions/shape of the wiring/electrode layers such as length/width, pad/island area, thickness, etc. of in chip packaging and interconnection technology art to achieve the desired electrical resistance and bonding yield.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select one of the second conductive path in the form of an island to improve the desired electrical resistance and bonding yield in Fukutomi et al's device.

Regarding claim 5, Fukutomi et al further disclose the insulating/bonding material (68/66 in Fig. 22 g) being provided between the wiring extended to the rear surface of the chip.

Regarding claim 9, Fukutomi et al further disclose the conductive paths made of a conductive foil/sheet selected from conventional material such as copper, nickel, etc. (Col. 22, line 33) but fail to specify selecting the conductive foil from a group consisting of aluminum and iron-nickel.

It is conventional in chip packaging and interconnection technology art to form conductive path/pattern using material such as copper, aluminum, etc. to achieve the desired electrical resistance.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive paths made of a conductive foil/sheet selected from a group consisting of copper, aluminum and iron-nickel to achieve the desired electrical resistance in Fukutomi et al's device.

8. Claims 8, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al (US Pat. 5976912) in view of Fjelstad (US Pat. 6001671) and Kweon et al (US Pat. 5900676).

Regarding claim 8, Fukutomi et al disclose forming the wiring patterns/islands using conventional photo resist processing (Col. 22, line 33; Col. 23, line 55) but fail to specify the side of each of the conductive paths being curved to mate with the insulating resin.

Fjelstad teaches forming curved sides of conductive wiring/paths mating with the insulating resin (Fig. 7E-7G; Col. 8) to improve the resin adhesion and bonding.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the side of each of the conductive paths being curved to mate

with the insulating resin to improve the resin adhesion and bonding using Fjelstad's wiring design in Fukutomi et al's device.

Regarding claim 12, Fukutomi et al further disclose forming the conductive solder patterns/bumps for mounting the devices on external wiring/mounting board but fail to specify the same for the first conductive path.

Kweon et al teach conventional mounting of the die pad/first conductive path having solder plated conductive pattern (150 in Fig. 13-15) on a wiring/mounting board (300 in Fig. 14; Col. 7, line 1-20) having corresponding conductive pattern.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to couple the first conductive path with a conductive pattern formed on the mounting board through a conductive layer to achieve the improved heat dissipation and an external connection using Kweon's mounting structure in Fukutomi et al's device.

Regarding claim 13, as explained above for claims 1 and 3, Fukutomi et al disclose forming the wiring patterns/islands and external connecting pads using conventional photo resist processing and solder printing (Col. 22, line 33; Col. 23, line 55) but fail to specify the conductive island of the second conductive path being a test pin.

Kweon et al teach forming the second conductive pad/path in the form of a conventional pin/lead or column (24 Fig. 3, 15, etc.) to provide an electrical connection, testing and external connection requirements for the assembly.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive island of the second conductive path as a test pin to achieve the electrical testing and rework capability using Kweon's pad structure in Fukutomi et al's device.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

01-03-02

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800